IN THE CLAIMS:

13. (Canceled).

14. (Canceled).

15. The semiconductor wafer of claim 3, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

16. The semiconductor wafer of claim 4, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

17. (Canceled).

18. (Canceled).

19. (Canceled).

20. (Canceled).

21. (Canceled).

22. (Canceled).

23. (Canceled).

24. (Canceled).

25. The semiconductor wafer of claim 1, wherein said bump electrodes are arranged in a grid array.

26. The semiconductor wafer of claim 2, wherein said bump electrodes are arranged in a grid array.

27. The semiconductor wafer of claim 3, wherein said bump electrodes are arranged in a grid array.

28. The semiconductor wafer of claim 4, wherein said bump electrodes are arranged in a grid array.

29. The semiconductor wafer of claim 1, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

30. The semiconductor wafer of claim 2, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

31. The semiconductor wafer of claim 3, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

32. The semiconductor wafer of claim 4, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.